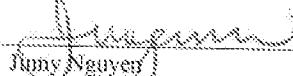


CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the USPTO-EFS-Web to Examiner John J. Tabone, Jr. on June 21, 2006.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Date: June 21, 2006

Robert T. BAILIS et al.

Confirmation No: 5286

Serial No: 10/016,449

Group Art Unit: 2138

Filed: December 10, 2001

Examiner: John J. Tabone, Jr.

Title: METHOD AND SYSTEM FOR USE OF A FIELD PROGRAMMABLE GATE ARRAY (FPGA) FUNCTION WITHIN AN APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) TO ENABLE CREATION OF A DEBUGGER CLIENT WITHIN THE ASIC

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REPLY TO OFFICE ACTION DATED APRIL 27, 2006

In response to the Final Office Action dated April 27, 2006, please amend the application as indicated on the following pages:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 6 of this paper.